In the Specification:

Please amend the paragraph beginning on page 2, line 1, as follows:

The above-mentioned self-align dual damascene process is mainly used for forming a bit line, a word line and a metal interconnection line of a dynamic random access memory (DRAM). Specially, by the self-align dual damascene process for forming the trench, a via hole used to form a via connecting upper and lower interconnection lines, may be formed simultaneously. By the self-align dual damascene process, a height difference due to interconnection lines may not be generated, since the via and interconnection lines are buried in interlayer insulating layers.

Please amend the paragraph beginning on page 3, line 26, as follows:

As shown in Fig. 2A, after forming the trench by etching the fourth interlayer insulating layer 18, the etching stop layer 17 is left except the via hole region. The etching stop layer 17 is usually formed with the nitride layer having a high capacitance value, in this case, a problem of capacitance increase ~~is occurred~~ occurs due to the remaining etching stop layer 17.

Please amend the paragraph beginning on page 7, line 29, as follows

After forming the fourth interlayer insulating layer 41, a photoresist layer is coated on the fourth interlayer insulating layer 41, and a trench mask 42 is formed by exposing and developing the photoresist layer. At this time, the width d_2 of the trench defined by the trench mask 42 is narrower than ~~that of the via hole, that is spacing between~~ the width d_1 of the photoresist pattern 40 (see Fig. 3C) to form the etching stop ~~layer patterns~~ pattern 37a.

Please amend the paragraph beginning on page 8, line 11, as follows:

After removing the trench mask 42, a metal layer is deposited on the resulting structure, and an etch back or a chemical mechanical polishing (CMP) is performed until the surface of the fourth interlayer insulating layer ~~36~~ 41 is exposed to form a metal interconnection line 43 in the trench, ~~ant~~ and at the same time a via 43a, connecting the metal interconnection line 43 to the metal interconnection line 35, is formed in the via hole 39.

Please amend the paragraph beginning on page 8, line 19, as follows:

The metal interconnection lines 35 and 43 and the via 43a may be formed with any one selected from the group consisting of Al, Cu, Au, Ag and Cr. The metal layers are deposited at a thickness ranging from about 2000 Å to about 30000 Å by using any one selected the group consisting of a chemical vapor deposition (CVD), ~~an~~ and electroless deposition and a physical vapor deposition (PVD).

Please amend the paragraph beginning on page 8, line 26, as follows:

Meanwhile, before forming the metal interconnection line 43, a diffusion barrier layer may be formed at a thickness ranging from about 1000 Å to about 5000 Å. The diffusion barrier layer is formed with any one selected from the group consisting of a TiN layer, a Ti layer, a W layer, a WN layer and a TiW layer ~~is deposited~~.

Please amend the paragraph beginning on page 9, line 5, as follows:

~~The disclosed method may prevent increasing of a capacitance value by remaining an etching stop layer for forming trench and decreasing etching target by etching a interlayer insulating layer where a void is already formed, so that a margin of a trench etching process may be maximized.~~ Since the minimum etching stop layer for forming the trench is used by patterning the etching stop layer to remain in inlet of the via hole, increase of capacitance due to the etching stop layer having high capacitance can be prevented. Also, since the interlayer insulating layer having a void is etched to form the trench, a margin of a trench etching process may be maximized.